

# DATA SHEET

## **74F2240**

Octal inverter buffer with  $30\Omega$  equivalent output termination (3-State)

## **74F2241**

Octal buffer with  $30\Omega$  equivalent output termination (3-State)

Product specification

1990 Dec 13

IC15 Data Handbook

# Octal buffers

# 74F2240, 74F2241

## FEATURES

- Octal bus interface
- 30Ω output termination ideal for driving DRAM
- 15mA source current

## DESCRIPTION

The 74F2240 and 74F2241 are octal buffers that are ideal for driving dynamic DRAM with impedance matching. The outputs are all capable of sinking 5mA and sourcing up to 15mA. The device features two output enables, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F2240	4.3ns	37mA
74F2241	4.5ns	30mA

## ORDERING INFORMATION

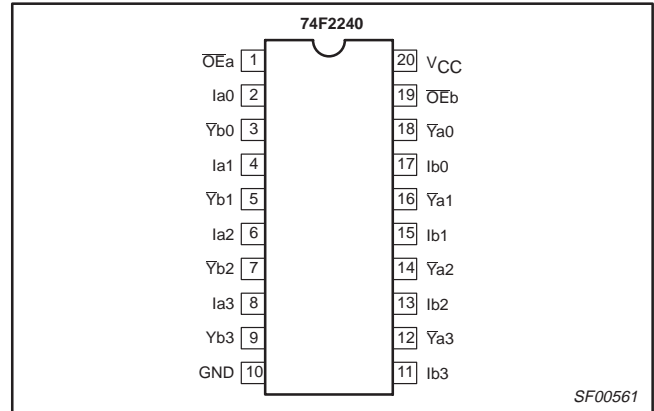
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	
20-pin plastic DIP	N74F2240N, N74F2241N	SOT146-1
20-pin plastic SOL	N74F2240D, N74F2241D	SOT163-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

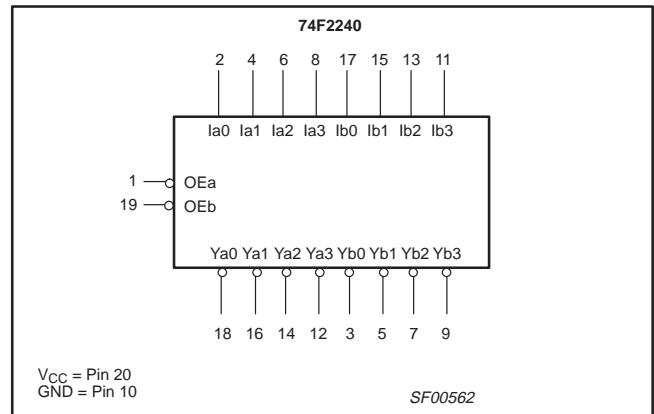
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I <sub>an</sub> , I <sub>bn</sub>	Data inputs	1.0/0.33	20μA/0.2mA
$\overline{OE}a$ , $\overline{OE}b$	Output enable inputs (active Low)	1.0/0.33	20μA/0.2mA
OE <sub>b</sub>	Output enable input (74F2241)	1.0/0.33	20μA/0.2mA
Y <sub>an</sub> , Y <sub>bn</sub>	Data outputs (74F2241)	750/8.33	15mA/5mA
Y <sub>an</sub> , Y <sub>bn</sub>	Data outputs (74F2240)	750/8.33	15mA/5mA

**NOTE:** One (1.0) FAST unit load is defined as: 20μA in the High state and 0.6mA in the Low state.

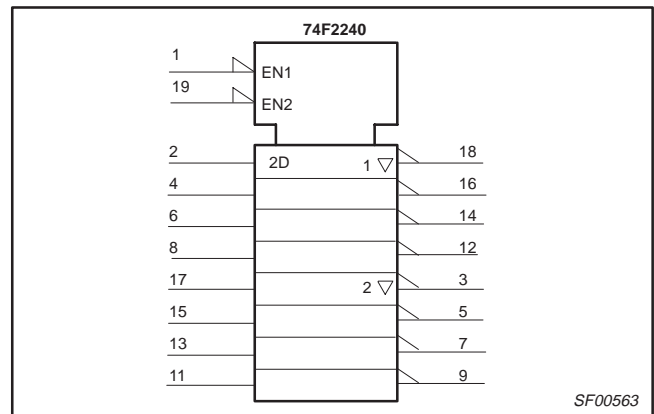
## PIN CONFIGURATION



## LOGIC SYMBOL



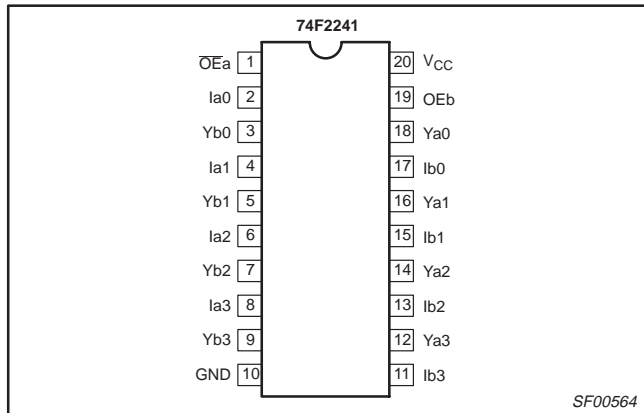
## IEC/IEEE SYMBOL



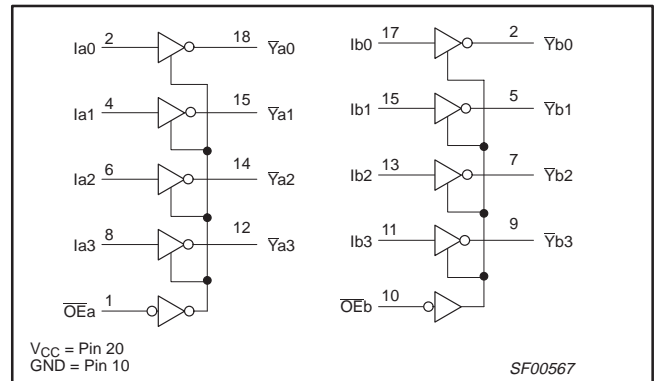
# Octal buffers

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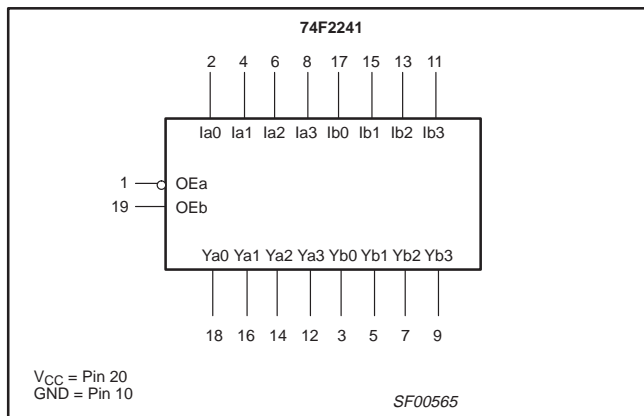
## PIN CONFIGURATION



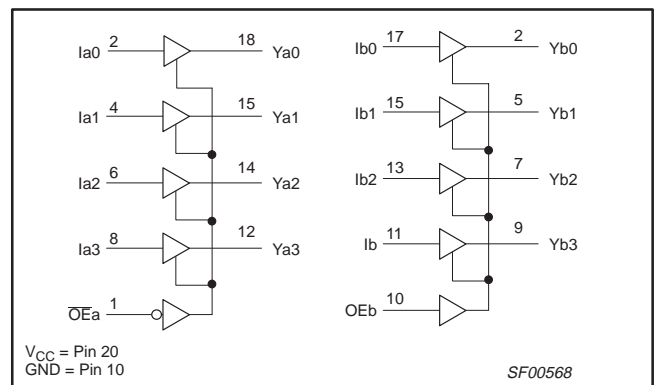
## LOGIC DIAGRAM FOR 74F2240



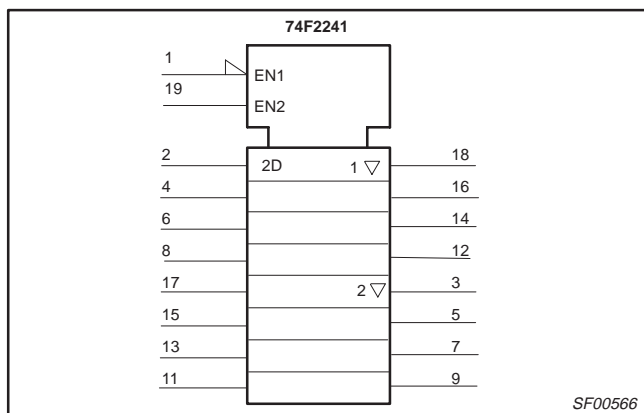
## LOGIC SYMBOL



## LOGIC DIAGRAM FOR 74F2241



## IEC/IEEE SYMBOL



## FUNCTION TABLE FOR 74F2240

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Yā	Yb̄
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

### Notes to function table for 74F2240

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

## FUNCTION TABLE FOR 74F2241

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

### Notes to function table for 74F2241

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

## Octal buffers

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in high output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in low output state	10	mA
$T_{amb}$	Operating free air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{Ik}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			5	mA
$T_{amb}$	Operating free air temperature range	0		+70	°C

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT
						MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>C</sub>	2.4			V	
				±5%V <sub>CC</sub>	2.7	3.4		V	
			I <sub>OH</sub> = -15mA	±10%V <sub>C</sub>	2.0			V	
				±5%V <sub>CC</sub>	2.0			V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN,	I <sub>OL</sub> = MAX	±10%V <sub>C</sub>			0.50	V	
				±5%V <sub>CC</sub>		0.42	0.50	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V					100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-0.2	mA	
I <sub>ozH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					50	μA	
I <sub>ozL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-60		-150	mA	
I <sub>CC</sub>	Supply current (total)	74F2240	I <sub>CCH</sub>	V <sub>CC</sub> = MAX		25	35	mA	
			I <sub>CCL</sub>			53	75	mA	
			I <sub>CCZ</sub>			35	45	mA	
		74F2241	I <sub>CCH</sub>			19	30	mA	
			I <sub>CCL</sub>			45	65	mA	
			I <sub>CCZ</sub>			27	40	mA	

**NOTES:**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
3. Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

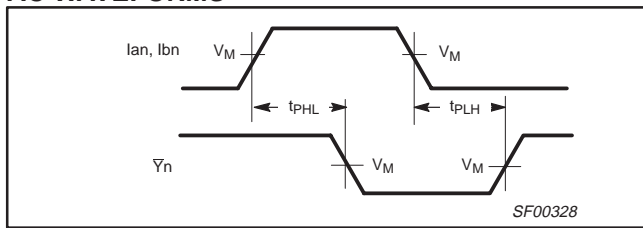
**AC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT	
				T <sub>amb</sub> = +25°C			T <sub>amb</sub> = 0°C to +70°C			
				V <sub>CC</sub> = +5.0V			V <sub>CC</sub> = +5.0V ± 10%			
				C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to Y <sub>n</sub>	74F2240	Waveform 1	3.0	5.0	7.0	2.5	8.0	ns	
t <sub>PZH</sub> t <sub>PZL</sub>			Output enable time to high or low level	Waveform 3	3.0	4.5	7.0	2.5	8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level		Waveform 4	3.5	5.0	8.0	3.0	9.0	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to Y <sub>n</sub>		74F2241	Waveform 3	2.0	3.5	6.5	1.5	7.0	ns
				Waveform 4	1.0	2.5	5.5	1.0	5.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level			Waveform 2	3.0	4.5	7.0	2.5	8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level	Waveform 3		3.0	5.0	7.0	2.0	8.0	ns	
		Waveform 4		3.5	5.5	7.5	3.0	8.5	ns	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level	Waveform 3		2.0	4.0	6.0	1.5	7.0	ns	
		Waveform 4	1.5	3.5	6.0	1.0	6.5	ns		

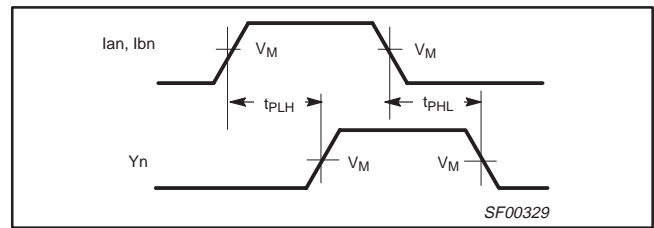
# Octal buffers

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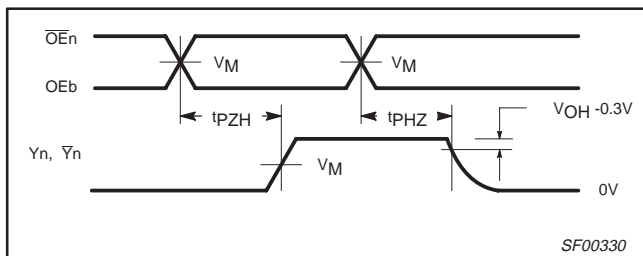
## AC WAVEFORMS



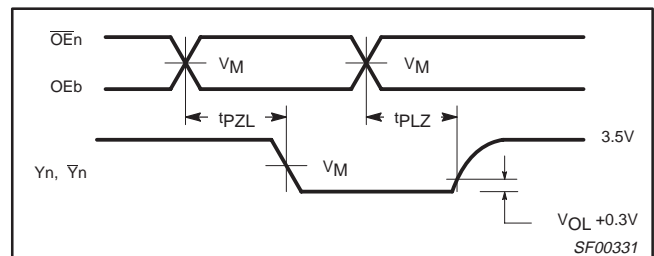
Waveform 1. Propagation delay for inverting outputs



Waveform 2. Propagation delay for non-inverting outputs



Waveform 3. 3-state output enable time to high level and output disable time from high level



Waveform 4. 3-state output enable time to low level and output disable time from low level

### NOTES:

For all waveforms,  $V_M = 1.5V$ .

The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Open Collector Outputs**

**Input Pulse Definition**

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**  
 $R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

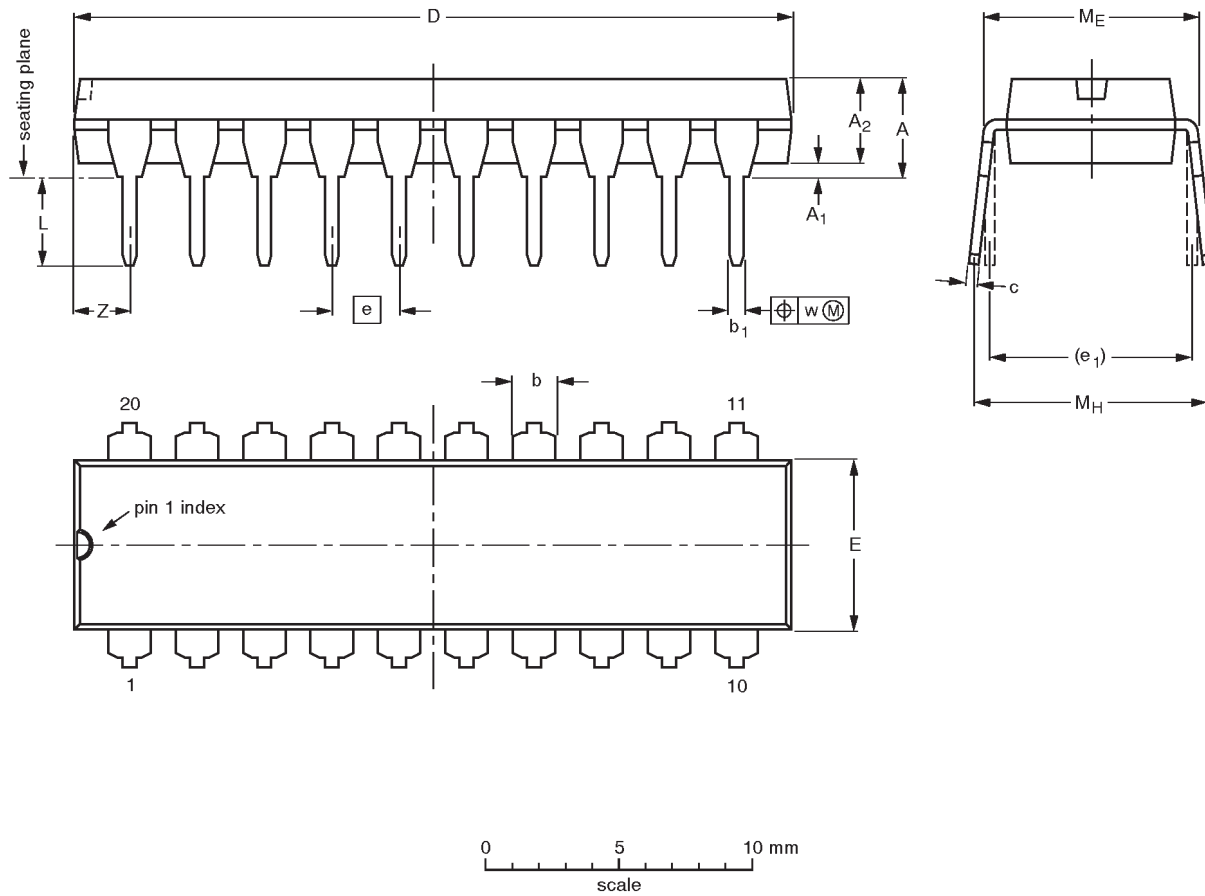
SF00128

# Octal buffers

74F2240/74F2241

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal buffers

## 74F2240/74F2241

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22



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Octal buffers

74F2240/74F2241

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**NOTES**

## Octal buffers

74F2240/74F2241

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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